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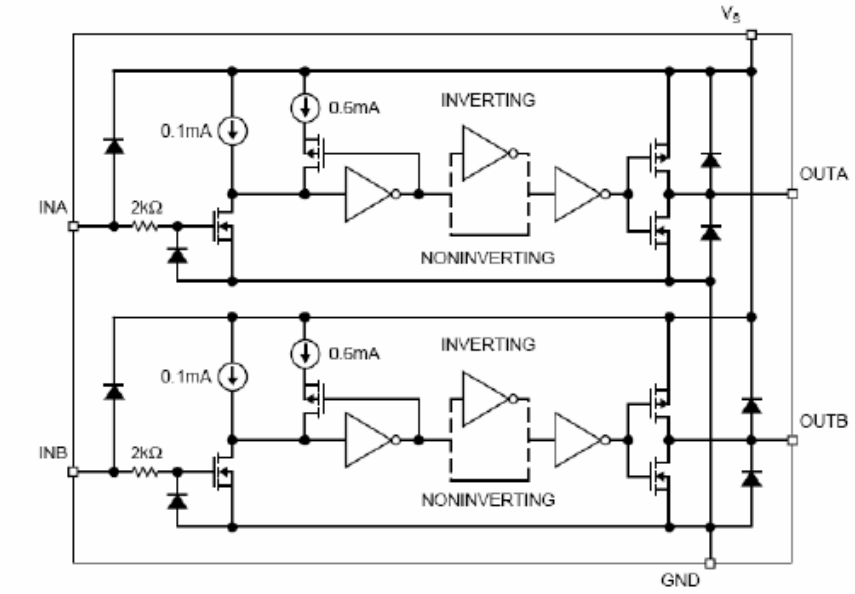
DL8132A

Features

- Bipolar/CMOS/DMOS construction
- Latch-up protection to >500mA reverse current
- 1.5A-peak output current
- 4.5V to 18V operating range
- Low quiescent supply current
  4mA at logic 1 input
  400uA at logic 0 input
- Switches 1000pF in 25ns
- Matched rise and fall times
- 7Ω output impedance
- <40ns typical delay
- Logic-input threshold independent of supply voltage
- Logic-input protection to -5V
- 6pF typical equivalent input capacitance
- 25mV max. output offset from supply or ground
- Dual inverting, dual noninverting, and inverting/noninverting configurations
- ESD protection

Functional Diagram



* All specs and applications shown above subject to change without prior notice.
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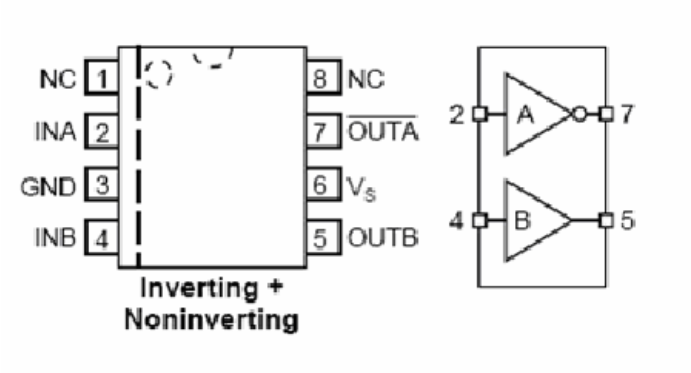
Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1,8	NC	Not internally connected
2	INA	Control input A: TTL/CMOS compatible logic input
3	GND	Ground
4	INB	Control input B: TTL/CMOS compatible logic input
5	OUTB	Output B: CMOS totem-pole output
6	V_S	Supply input: +4.5V to +18V
7	OUTA	Output A: CMOS totem-pole output

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_S)……..……..……..+22V
Input Voltage (V_{IN})……VS +0.3V to GND -5V
Junction Temperature (T_J) ……+150℃
Storage Temperature ……..-65℃ to +150℃
Lead Temperature (10 sec.)……300℃
ESD Rating , Note 3

Operating Ratings (Note 2)

Supply Voltage (V_S)……..+4.5V to +18V
Temperature Range (T_A) ……..-40℃ to +85℃
Package Thermal Resistance
SOIC θ JA ……120℃/W
SOIC θ JC ……75℃/W

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Electrical Characteristics

4.5V≦V_S≦18V; T_A =25℃, bold values indicate full specified temperature range ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input						
V_{IH}	Logic 1 Input Voltage		2.4 2.4	1.4 1.5	- -	V V
V_{IL}	Logic 0 Input Voltage		- -	1.1 1.0	0.8 0.8	V V
I_{IN}	Input	0≦V_{IN}≦V_S	-1	-	1	uA
Output						
V_{OH}	High Output Voltage		VS -0.025	- -	- -	V
V_{OL}	Low Output Voltage		-	-	0.025	V
R_O	Output Resistance	I_{OUT}=10mA, V_S=18V	- -	6 8	10 12	Ω Ω
I_{PK}	Peak Output Current		-	1.5	-	A
I	Latch-Up Protection	With stand reverse current	-	>500	-	mA
Switching Time						
t_R	Rise Time	Test Figure 1	- -	18 20	30 40	ns
t_F	Fall Time	Test Figure 1	- -	15 29	20 40	ns
t_{D1}	Delay Time	Test Figure 1	- -	17 19	30 40	ns
t_{D2}	Delay Time	Test Figure 1	- -	23 27	50 60	ns
t_{PW}	Pulse Time	Test Figure 1	400	-	-	ns
Power Supply						
I_S	Power Supply Current	V_{INA}=V_{INB}=3.0V	- -	1.4 1.5	4.5 8	mA
I_S	Power Supply Current	V_{INA}=V_{INB}=0.0V	- -	0.18 0.19	0.4 0.6	mA

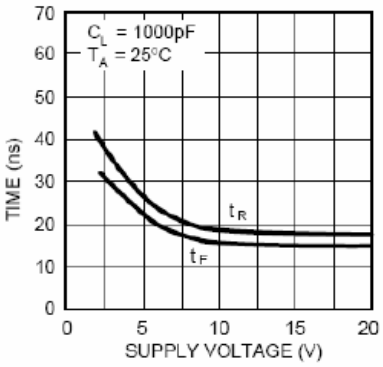
Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

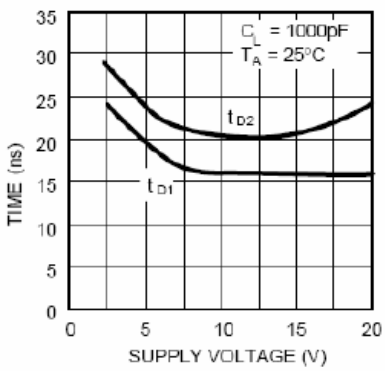
Note 3. Devices are ESD sensitive. Handling precautions recommended.

Electrical Characteristics

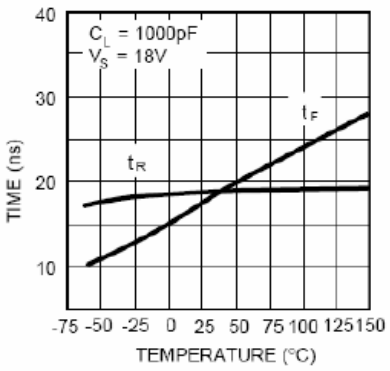
Rise and Fall Time vs. Supply Voltage



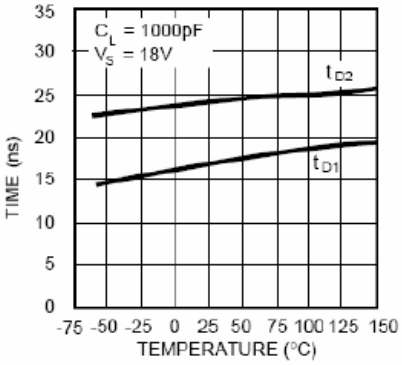
Delay Time vs. Supply Voltage



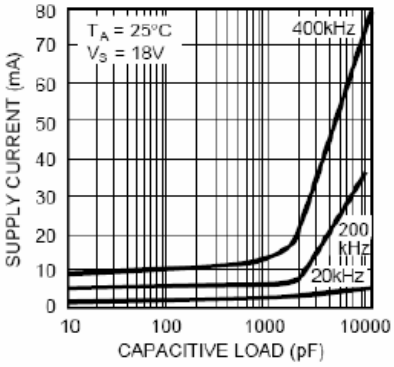
Rise and Fall Time vs. Temperature



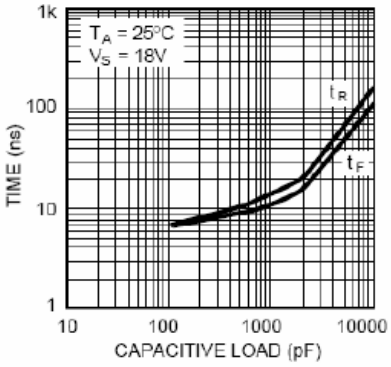
Delay Time vs. Temperature



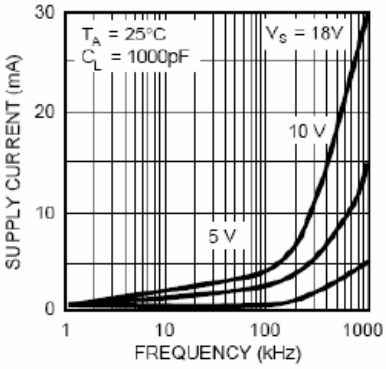
Supply Current vs. Capacitive Load



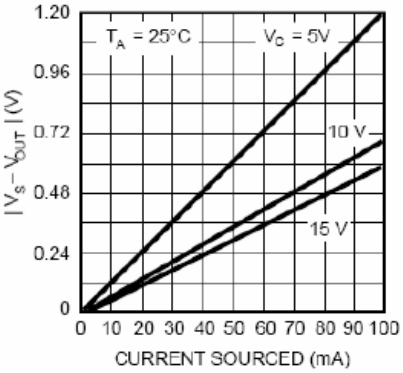
Rise and Fall Time vs. Capacitive Load



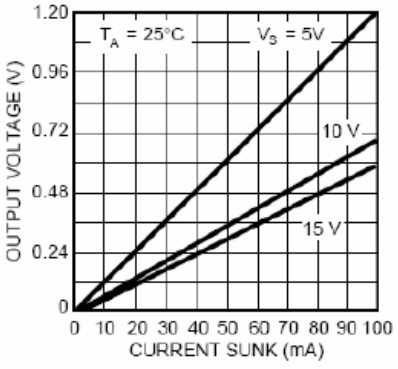
Supply Current vs. Frequency



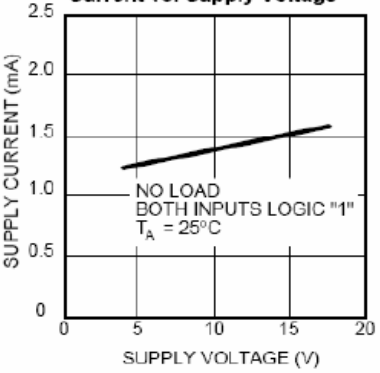
High Output vs. Current



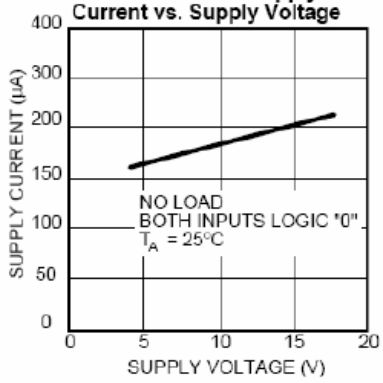
Low Output vs. Current



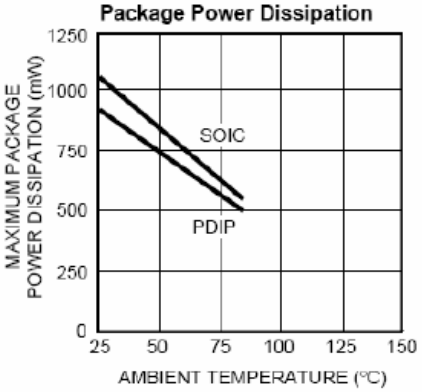
Quiescent Power Supply Current vs. Supply Voltage



Quiescent Power Supply Current vs. Supply Voltage



Package Power Dissipation



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Applications Information

Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000pF load by 16V in 25ns requires 0.8A from the supply input.

To guarantee low supply impedance over a wide frequency range, parallel capacitors are recommended for power supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5”) should be used. A 1.0uF film capacitor in parallel with one or two 0.1uF ceramic MLC capacitors normally provides adequate bypassing.

Grounding

When using the inverting drivers in the DL8132A , individual ground returns for the input and output circuits or a ground plane are recommended for optimum switching speed.

The voltage drop that occurs between the driver’s ground and the input signal ground, during normal high-current switching, will behave as negative feedback and degrade switching speed.

Control Input

Unused driver inputs must be connected to logic high (which can be V_S) or ground. For the lowest quiescent current (<500uA), connect unused inputs to ground. A logic-high signal will cause the driver to draw up to 9mA.

The drivers are designed with 100mV of control input hysteresis. This provides clean transitions and minimizes output stage current spikes when changing states. The control input voltage threshold is approximately 1.5V. The control input recognizes 1.5V up to V_S as a logic high and draws less than 1uA within this range.

Power Dissipation

Power dissipation should be calculated to make sure that the driver is not operated beyond its thermal ratings. Quiescent power dissipation is negligible. A practical value for total power dissipation is the sum of the dissipation caused by the load and the transition power dissipation (P_L+P_T).

Load Dissipation

Power dissipation caused by continuous load current (when driving a resistive load) through the driver’s output resistance is:

$$P_L = I_L^2 R_O$$

For capacitive loads, the dissipation in the driver is:

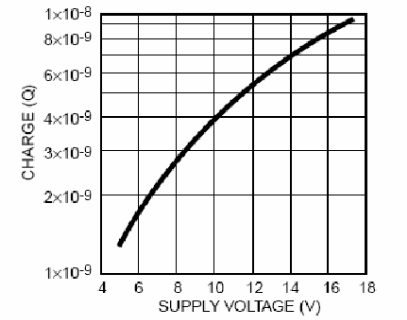
$$P_L = f C_L V_S^2$$

Transition Dissipation

In applications switching at a high frequency, transition power dissipation can be significant. This occurs during switching transitions when the P-channel and N-channel output FETs are both conducting for the brief moment when one is turning on and the other is turning off.

$$P_T = 2fV_SQ$$

Charge (Q) is read from the following graph:



Crossover Energy Loss per Transition

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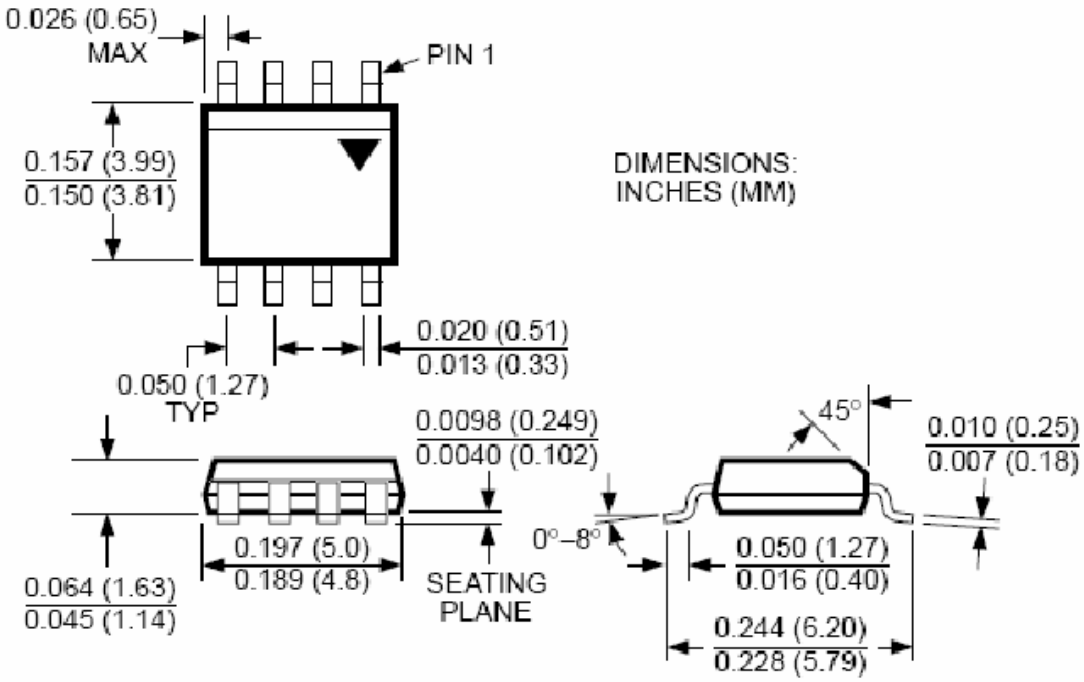
Package Information



8-Lead SOP (M)

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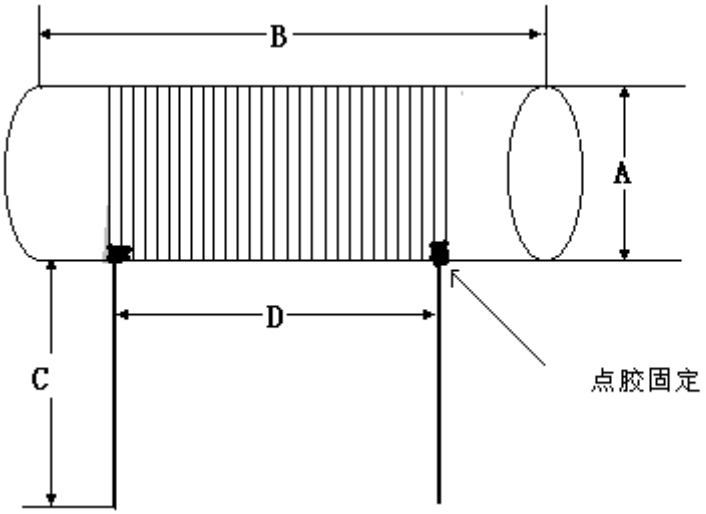
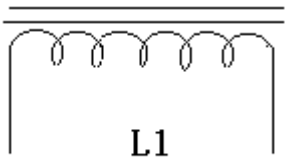
规 格 书

客户名称：	产品名称：磁棒线圈	产品规格：5*30/160T-2*35
产品编号：LS200924	记录编号：№00	日期：2009.05.25

1 产品尺寸



2 产品电路图



3 产品数据表

磁 芯	5*30	材 质	铁氧体磁芯	
磁芯尺寸	A	5	B	30
引脚长度	C	35±5	D	18±5
引 脚	E		F	
绕线线规	QA-0.10		匝数	160T
L 电感量	690UH0% 1KHZ			
备 注				

设 计：	画 图：	审 核：	客户确认：

深圳市晶峰达电子科技有限公司
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DL8132C PKE 控制专用芯片

简介

DL8132C 是供 PKE 防盗器专用的遥控器 IC,内含 LF(Low frequency 125KHz) OOK 接收电路及逻辑解码电路,以及 4 组按键输入,可控制外部 UHF 315/433MHz 发射电路编码

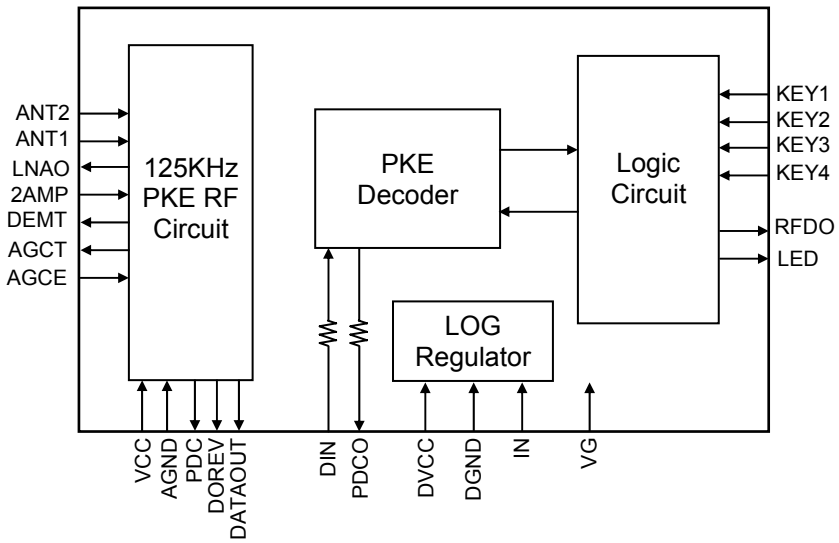
特点

◎ 工作电压范围:2.2V~5V
◎ 宽的动态范围: 90 db
◎ 高灵敏度: 30uV
◎ 低功率消耗:
工作模式(Stand By): 8uA
LF 解码模式:25uA
Tx 编码模式:100~200uA
◎ 只需少许外部组件
◎ 内建 8 Bit 125K Wakeup ID
◎ 内建 20 Bit UHF ID (100 万组)
◎ 外接 4 组按键输入

应用范围

◎ PKE 防盗器系统遥控器 IC

方块图



供货封装规格

芯片型号	封装形式
DL8132C	24 Pin SSOP

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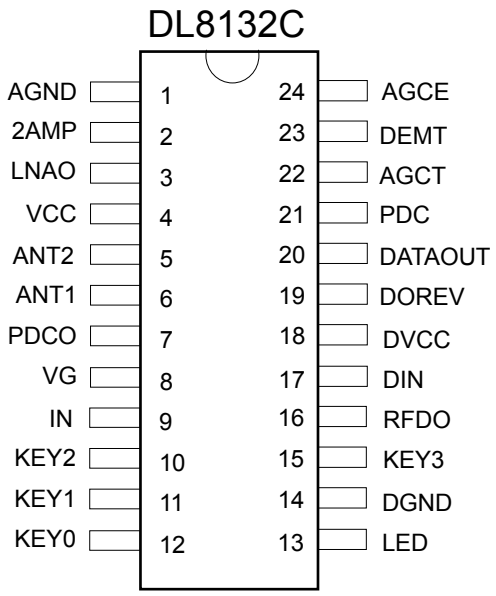
(以上电路及规格仅供参考,本公司得径行修正)

引脚图



管脚说明

引脚序号	管脚名称	说　　明
1	AGND	模拟地。
2	2AMP	第二级放大器输入脚。
3	LNAO	LNA 输出脚。
4	VCC	模拟电源输入脚。
5	ANT2	差动输入天线端 2。
6	ANT1	差动输入天线端 1。
7	PDCO	数字端控制 RF 电路电源输出脚。
8	VG	预设接 DVCC(High)。
9	IN	预设接 DVCC(High)。
10	KEY2	按键输入脚。
11	KEY1	按键输入脚。
12	KEY0	按键输入脚。
13	LED	状态灯号输出脚。
14	GND	数位地。
15	KEY3	按键输入脚。
16	RFDO	UHF(315/433)串行编码输出脚。
17	DIN	解调数据输入脚。
18	DVCC	数字端电源输入脚。
19	DOREV	互补式输出级输出脚。
20	DATAOUT	互补式输出级输出脚。
21	PDC	RF 状态控制输入脚。此脚接地 RF 部分将动作;此脚接 VCC,RF 部分将进入休眠模式。
22	AGCT	自动增益控制时间补偿电容输出脚。
23	DEMT	OOK 解调时间补偿电容输出脚。
24	AGCE	自动增益控制致能输入脚。平常接至 VCC。

RF 功能叙述

天线端的连接经由 ANT1 和 ANT2 进入到 RF, 高感度,天线电路的 Q 值要尽量提高. ANT1、ANT2 在差动模式下的输入阻抗为 400KΩ 在单端模式下的输入阻抗为 200KΩ.一个带通滤波器电路应接在 LNAO 和 2AMP 之间. LNAO 输出阻抗为 75KΩ,以及 2AMP 输入阻抗为 150KΩ.

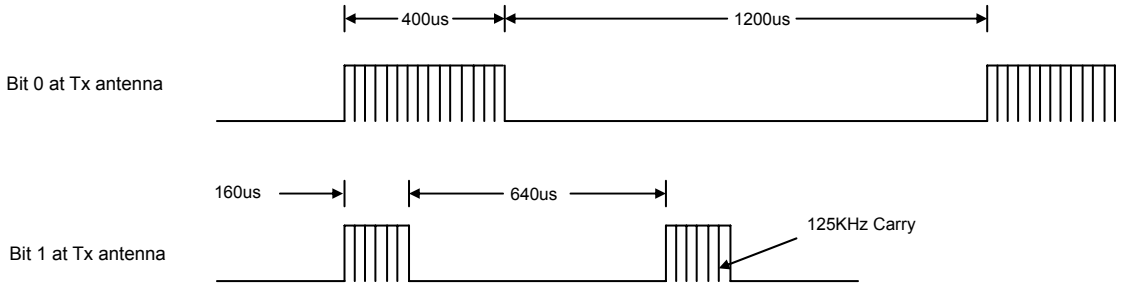
解调输出电路(DEMT)需外接电容以确保解调功能正常,电容值依照传送数据的速率来决定,通常数值在 100pF 到 10nF 之间.将 AGCE 接 VCC 时为一般模式,将 AGCE 接 GND 为致能模式此时 AGCE 增益设为最大.

自动增益控制(AGC)检测器输出端(AGCT)需要外接电容因它会影响 AGC 峰值检测的功能,这电容数值会影响 AGC 峰值检测的反应速度.

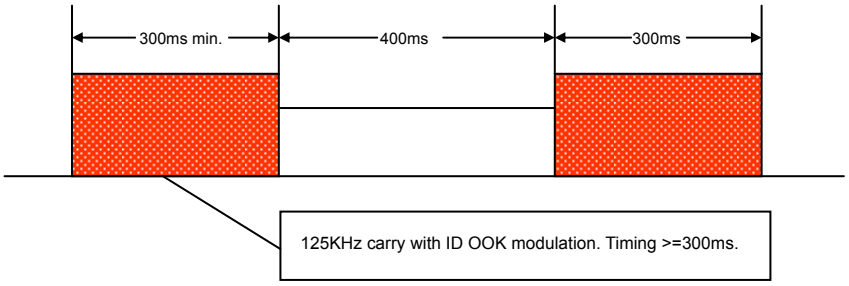
如果 PDC 脚被接到 VDD, RF 电路将进入休眠状态.

LF (125KHz)数据编码格式:

1. 数据格式:



2. 资料基本格式定义(16 Bits): 5(H)(前导码) + (8 bit ID)(先送 MSB BIT) + F(H) (结束码), 此 ID 数据封包必需连续重复送出, 封包与封包之间不可间断.
   UHF Data/Function Code(自动回答码): 1011
3. 8 bit ID : 是以序号码 20 Bit,低位元 8 bit 为 LF Wake up ID
4. 逻辑 0 总周期: 1600 us +/- 10%, 逻辑 High 周期: 400 us +/- 10%.
5. 逻辑 1 总周期: 800 us +/- 10%,逻辑 High 周期: 160us +/- 10%.
6. 发射端周期图:



地址码编码格式:

Code Word Format

DL8132C 发射编码基本包括下列 3 部分如下图示,各部定义如下所述:

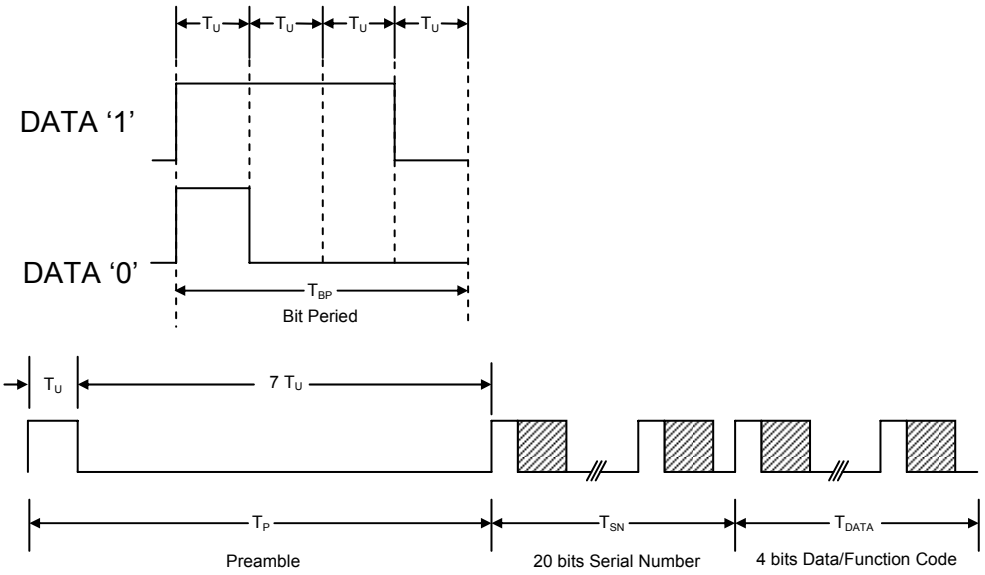
Preamble: 发设前置码,共 8 基本周期.

Serial Number: 序号码 20 Bit,低位元 8 bit 为 LF Wake up ID.

Data/Function: 数据功能码,4 Bit.

发码时以 LSB 先送出.

Preamble	Serial Number	Data/Function
8 T	20 bits (80T)	4 bits (16T)



Symbol	Parameter	Min.	Typ.	Max.	Unit	Remarks
T_U	Unit Time	140	200	260	uS	
T_P	Preamble	1.12	1.6	2.08	mS	$8*T_U$
T_{SN}	20 bits serial number	11.2	16	20.8	mS	$80*T_U$
T_{DATA}	4 bits data/function code	2.24	3.2	4.16	mS	$16*T_U$
Total	Total time of code word	14.6	20.8	27.0	mS	$104*T_U$

数据编码格式:

Data/Function Code				KEY & Handset Status			
D0	D1	D2	D3	KEY0	KEY1	KEY2	KEY3
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Data/Function Code(自动回答码): 1011

极限参数（Ta=25℃）

参数	符号	数值	单位
供应电压	V_{CC}	5.5	V
工作温度范围	Range Tamb	-20 to +85	℃
储存温度范围	Range Rstg	-40 to +120	℃

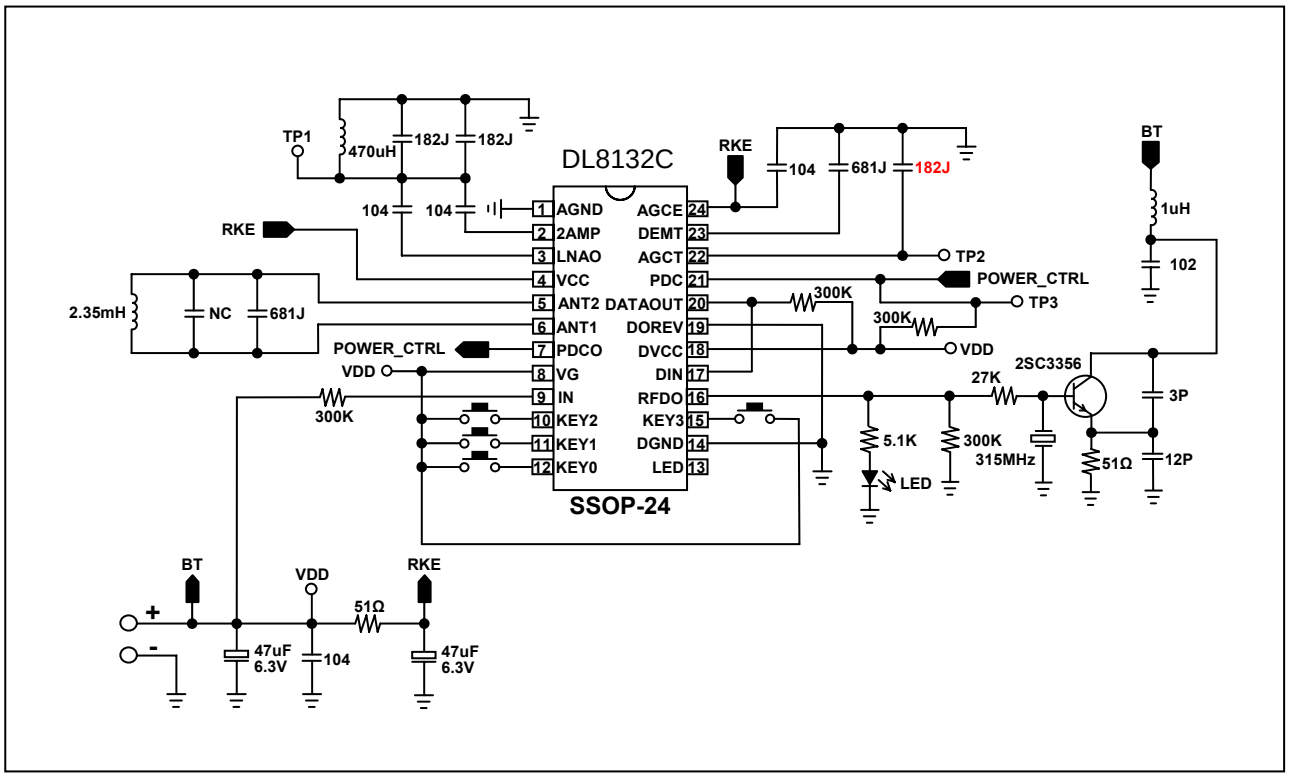
说明

器件的负荷不得超出“最大极限值”中所列出的范围，否则器件可能永久性损坏，也不允许在临界值下负荷过久，这样即使不损坏器件，也可能影响其可靠性。

电气参数（除非特殊说明,T_{EMP}=25℃, V_{DD}=3.0V）

参数	测试条件	符号	最小值	一般值	最大值	单位
工作电压范围	Pad/Pin V_{CC}	V_{CC}	2.2	-	5.5	V
工作消耗电流(LF 解码模式)	Pad/Pin V_{CC}	I_{CC}	16	25	35	μA
工作消耗电流(Standby 模式)	Pad/Pin V_{CC}	I_{CC}	6	8	10	μA
工作消耗电流(Tx 编码模式)	Pad/Pin V_{CC}	I_{CC}	100	135	200	μA
RF 传感器睡眠模式耗电			-	< 1uA	-	μA
频率接收范围		Fin	100	-	240	KHz
最小输入电压(最高灵敏度)	Pad/Pin ANT1, ANT2	Vin	20	30	40	μV
输出电压(OUT 1 low) 外部电路接成 NPN 开级级模式	V_I = 100μV I_{OUT1} L = 30μA	V_{OUT1} L	-	-	0.3	V
输出电压(OUT 2 high) 外部电路接成 PNP 开级级模式	V_I = 100 μV I_{OUT2} H = 30μA	V_{OUT2} H	Vcc- 0.5	Vcc -0.3	-	V
输出电流 (OUT 1 high) 外部电路接成 NPN 开级级模式	V_I = 100μV 100% amplitude	I_{OUT1} H	-	-	1	μA
输出电流(OUT 2 low) 外部电路接成 PNP 开级级模式	V_I = 100μV 100% amplitude	- I_{OUT2} L	-	-	1	μA

遥控器原理图



注: DL8132C 除 AGCT(PIN 22)外围电容值改为 1.8nF, 功能及特性皆与 DL8132C相同, 主板及主程序皆不用修改.

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CUST. NAME		DATE	
DESCRIPTION	Power Choke Inductors	TYPE	
GS PART NO.	DL8132B-1250-102M	DWG. NO.	031818
CUST. PART NO.		GS SAMPLE NO.	073652

Material List

No.	Item	Supplier	Material
1	CORE	K008	DL3 AP 3×12×50
2	WIRE	F019	0.26Φ2UEW NY(自粘线) ×133Ts (Ref.)
3	TAPE		美纹胶带 20mm(宽) ×60 mm(长)
			美纹胶带 5mm(宽) ×55 mm(长)
4	EPOXY	CE014	2006AB
			Remark: Weight:11.66g

※ No Varnish.
※ 起、收线处需点 Epoxy 固定。
※ Winding: L Type